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09/857,673	01/17/2002	Manfred Leiter	10191/1840	9963

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EXAMINER

ZARNEKE, DAVID A

ART UNIT PAPER NUMBER

2827

DATE MAILED: 01/15/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application No.

09/857,673

Applicant(s)

LEITER ET AL.

Examiner

David A. Zarneke

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on 03 November 2003.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 22-46 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 22-46 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

## Priority under 35 U.S.C. §§ 119 and 120

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a) ☐ All b) ☐ Some \* c) ☐ None of:  
1. ☐ Certified copies of the priority documents have been received.  
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).  
\* See the attached detailed Office action for a list of the certified copies not received.
- 13) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.  
a) ☐ The translation of the foreign language provisional application has been received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

## Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892) 4) ☐ Interview Summary (PTO-413) Paper No(s). \_\_\_\_\_
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 5) ☐ Notice of Informal Patent Application (PTO-152)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) \_\_\_\_\_ 6) ☐ Other: \_\_\_\_\_

## **DETAILED ACTION**

### ***Response to Arguments***

Applicant's arguments with respect to claims 22-46 have been considered but are moot in view of the new ground(s) of rejection.

Applicant first argues (see page 6 & page 8 of response) that the newly added limitation "wherein the package substrate includes a thinned central area and a remaining thick substrate edge that stabilizes the package substrate and that is used for handling purposes" is not taught or suggested by the art of record, in neither Denlinger nor Giboney.

The examiner agrees this argument and cites a new rejection of the claims below.

Second, applicant argues that claims 26, 29-31, 33, 34, 36 & 37 (see page 7 of the response) and claims 41-44 (see page 9 of the response), which are rejected as subject matter containing subject matter that are obvious matters of design choice, are improperly rejected under 103 because the office action makes generalized unsupported assertions that reflect a subjective "obvious to try" standard and does not include proper evidence to support the obviousness rejection.

The examiner asserts that motivation is supplied for each claim. At the end of most of the design choice assertions is a statement was included providing further motivation for using each limitation. Regardless, each limitation is an obvious, well known in the art method of performing the recited step and is an acceptable design

choice used in the art to perform the technique claimed. Further support or explanation will now be provided for each claim.

Regarding claim 26, the use of photostructuring to form the cavities is an obvious matter of design choice because it increases the control and precision of pattern to be etched into the substrate.

With respect to claim 29, an explanation was included in the previous office action and is restated below.

As to claims 30 and 31, the use of metal to form the chip carrier is an obvious matter of design choice because metal is a conventional material used to form chip carriers. Metals provide strength and heat dissipation.

In re claim 33, the use of a Gunn diode is an obvious matter of design choice because Gunn diodes are conventionally known to be used because they generate high frequency electromagnetic waves useful in the production of radar waves.

Regarding claims 34 and 36, the use of a semiconductor material to form the cover substrate and cover layer is an obvious matter of design choice because it allows for contacting a component to a microstructured contact spring mounted on the side of the cover substrate ensuring permanent and reliable contacting of the component.

With respect to claim 37, using contact springs made by galvanic metal deposition is an obvious matter of design choice because galvanic metal deposition makes possible smaller dimensions of the contact spring, which because of the small dimensions of the electronic component, provide a great spring path.

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As to claim 41, the arranging of diodes on a carrier such that they align with the cavities in a package substrate is an obvious matter of design choice because one of any skill in the art realizes that the diodes must be aligned with the cavities, otherwise the package can not be completed when the package substrate is lowered onto the carrier.

In re claims 42 and 43, joining the cover substrate and cover layer to the package substrate, separating package into insulator structures and joining the component carrier layer to electronic components is an obvious matter of design choice because this are the next logical steps in the process. What else are you going to do with the carrier, cover substrate and cover layer? Of course you are going to join them together, form separate structures and join them to components.

Regarding claim 44, the use of selective etching to form the insulator structures is an obvious matter of design choice because selective etching only removes material at the required location, saving material costs and saving the materials not to be etched from degradation and possible weakening of these materials.

### ***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 22, 24, 26-33, 36, 37 and 40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Denlinger, US Patent 4,021,839, in view of Edwards et al., US Patent 4,266,334.

Denlinger discloses (see column 2, line 60 through column 3, line 42 and column 5, lines 34-43) a method of packaging electronic components, having the steps:

forming a plurality of cavities 15 in a package substrate 12, where the package substrate is made of a photopatternable glass (see column 3, lines 4-17, for example);  
mounting electronic components 20/22/24 in the cavities;

sealing the cavities with a cover substrate or cover layer 26; and  
separating the electronic components (Figure 4).

Denlinger fails to teach the limitation "wherein the package substrate includes a thinned central area and a remaining thick substrate edge that stabilizes the package substrate and that is used for handling purposes."

Edwards teaches thinned substrate imagers having a thinned central area and a remaining thick substrate edge that stabilizes the package substrate and that is used for handling purposes (figure 5) wherein the thick substrate edge "provides some stiffness and mechanical support for the relatively fragile thinned substrate region" (2, 59+).

Regarding claims 24, Denlinger teaches the attachment of an electrically conductive (3, 21+) base (16) to side opposite the cover substrate or cover layer.

Regarding claim 26, the use of photostructuring to form the cavities in the substrate is an obvious matter of design choice. Design choices and changes of size are generally recognized as being within the level of ordinary skill in the art (MPEP 2144.04(d)). Photostructuring is a commonly known in the art method of forming openings in substrates.

With respect to claim 27, Denlinger teaches the cavities as passing through the package substrate (figures).

As to claim 28, Denlinger teaches the cavities as being shallow to accommodate the electronic components (Figures).

With respect to claim 29, the arranging of the diodes on a carrier such that they align with the cavities is an obvious matter of design choice. Design choices and

changes of size are generally recognized as being within the level of ordinary skill in the art (MPEP 2144.04(d)). This would make the process quicker and easier since placing multiple diodes on a carrier is easier than placing them in an opening.

As to claims 30 and 31, the choosing of a metal (claim 30), such as silver (Ag) (claim 31), as the material of the carrier layer is an obvious matter of design choice. Design choices and changes of size are generally recognized as being within the level of ordinary skill in the art (MPEP 2144.04(d)). Metallic (Ag) chip carriers are commonly known in the art.

Regarding claim 32, Denlinger teaches the electronic components as being diodes (abstract).

Regarding claim 33, the choosing of a Gunn diode as the type of diode used is an obvious matter of design choice since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice (*In re Leshin* 125 USPQ 416). Gunn diodes are very commonly known in the art.

As to claims 36 and 37, the attaching a contact spring to the cover substrate or layer from contacting the electronic component is an obvious matter of design choice. Design choices and changes of size are generally recognized as being within the level of ordinary skill in the art (MPEP 2144.04(d)). Contact springs are a very well known in the art method of contacting components.

With respect to claim 40, Denlinger teaches the use of a saw to separate the electronic components (5, 34+).



Claims 23, 25, 34, 35, 38, 39 and 41-44 are rejected under 35 U.S.C. 103(a) as being unpatentable over Denlinger, US Patent 4,021,839, in view of Edwards et al., US Patent 4,266,334, as applied to claim 22 above, and further in view of Giboney et al., US Patent 6,351,027.

Regarding claim 23, Denlinger and Edwards both fail to teach the package substrate as being made of a Si semiconductor material.

Giboney (Figure 1) teaches a chip mounted enclosure for enclosing diodes (3, 39+) wherein the bottom piece (13) is made of silicon (3, 49+) and the side walls (21-24) can be made of a semiconductor material, such as Si (5, 11+ & 3, 49+), wherein the bottom piece (13) and sidewall pieces (21-24) form a cavity for placement of a diode (11), which is in turn covered by a top piece (15).

With respect to claims 34 and 35, Giboney teaches the use of a Si semiconductor material

As to claims 34 and 35, while Denlinger teaches the lid (26) to electrically conductive and specifically the use of Au-plated Cu, silicon is a known equivalent electrically conductive material as taught by Giboney (5, 11+).

The substitution of one known equivalent technique for another may be obvious even if the prior art does not expressly suggest the substitution. Ex parte Novak 16 USPQ 2d 2041 (BPAI 1989); In re Mostovych 144 USPQ 38 (CCPA 1964); In re Leshin 125 USPQ 416 (CCPA 1960); Graver Tank & Manufacturing Co. V. Linde Air Products Co. 85 USPQ 328 (USSC 1950).

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Regarding claims 25 and 38, Giboney teaches the cover as being made of glasses or ceramics (6, 5+).

With respect to claims 39, it would have been obvious to one of ordinary skill in the art at the time of the invention, as a matter of design choice, that if an organic dielectric was used as the lid, that to form an electrical connection an opening would have to be etched in the dielectric and then a metal layer would have to be applied. Further, the choice of the organic dielectric as being a photosensitive lacquer would also be a matter of design choice. Design choices and changes of size are generally recognized as being within the level of ordinary skill in the art (MPEP 2144.04(d)).

As to claim 41, Giboney teaches the package substrate (13) as an carrier layer having the diodes mounted thereon; forming the cavities as an insulator structure (20a-d) situated outside the package substrate and joining them together along with the cover substrate or layer (Figures 3A-E).

Giboney fails to teach the diodes as being mounted on a carrier and then mounted to the insulator structures and the cover substrate or layer.

It would have been obvious to one of ordinary skill in the art to arrange the diodes on a carrier such that they align with the cavities is an obvious matter of design choice. Design choices and changes of size are generally recognized as being within the level of ordinary skill in the art (MPEP 2144.04(d)). This would make the process quicker and easier since placing multiple diodes on a carrier is easier then placing them individually on the substrate.

Regarding claim 42, Giboney teaches joining a cover substrate or layer and the package substrate through the insulator structures.

It would have been obvious to one of ordinary skill in the art to arrange the diodes on a carrier such that they align with the cavities as an obvious matter of design choice. Design choices and changes of size are generally recognized as being within the level of ordinary skill in the art (MPEP 2144.04(d)). This would make the process quicker and easier since placing multiple diodes on a carrier is easier than placing them individually on the substrate.

With respect to claim 43, Giboney teaches applying the diodes to the package substrate; forming insulator structures and joining a cover substrate or layer to the package substrate (figures 3A-E).

It would have been obvious to one of ordinary skill in the art to deposit the diodes on the package substrate by arranging them on a carrier as an obvious matter of design choice. Design choices and changes of size are generally recognized as being within the level of ordinary skill in the art (MPEP 2144.04(d)). This would make the process quicker and easier since placing multiple diodes on a carrier is easier than placing them individually on the substrate.

As to claims 44, Denlinger teaches the package substrate as being a carrier made of glass (3, 4+), with separate insulator structures formed thereon (Figure 3).

Denlinger fails to teach the insulator structures as being exposed by selective etching.

It would have been obvious to one of ordinary skill in the art at the time of the invention to use selective etching to form the insulator structures as an obvious matter of design choice. Design choices and changes of size are generally recognized as being within the level of ordinary skill in the art (MPEP 2144.04(d)).

### ***Conclusion***

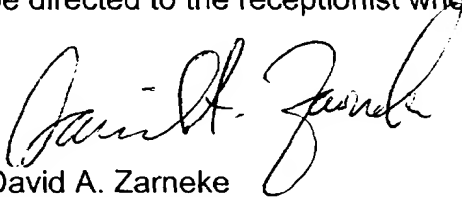
Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication from the examiner should be directed to David A. Zarneke at (703)-305-3926. The examiner can normally be reached on M-F 10AM-6PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamand Cuneo can be reached on (703)-308-1233. The fax

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phone number is (703)-872-9306. After February 5, 2004, the examiner's phone number will be (571)-272-1937 and his supervisor's phone number will be (571)-272-1937. Any inquiry of a general nature or relating to the status of this application should be directed to the receptionist whose telephone number is (703)-308-6789.

A handwritten signature in black ink, appearing to read "David A. Zarneke". The signature is fluid and cursive, with the first name "David" and last name "Zarneke" clearly distinguishable.

David A. Zarneke  
Primary Examiner  
January 7, 2004